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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/938,571 | 08/27/2001 | Koji Ono | 35.C15701 | 1644 |

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| EXAMINER |
|---|
| ORTIZ, EDGARDO |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 08/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

| Application No. | Applicant(s) |
|---|---|
| 09/938,571 | Ono |
| **Examiner** | **Art Unit** |
| Edgardo Ortiz | 2815 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on *May 28, 2002*

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) *1, 7, and 13-29* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideratio

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 7, and 13-29* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examine

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

This Office Action is in response to an amendment filed May 28, 2002 on which Applicant amended claims 1 and 7, canceled claims 2-6 and 8-12 and added new claims 13-29.

### *Drawings*

1. Figure 7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 15, 16, 22 and 23 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant fails to describe in the specification the structural basis for which the "wiring substrate", is produced as part of the final structure of the claimed invention. Thus, Applicant fails to properly disclose the enablement of the claimed invention.

*Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 7, 13, 19, 20, 26 and 27 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Hideki (Japanese Patent No. 08-241976) in view of Applicant's admitted prior art, as shown on figure 7. With regard to Claim 1, Hideki teaches a substrate (30), a solid-state image pickup element chip (32) on which a plurality of solid-state image pickup elements are mounted, said solid-state image pickup element chip being formed on said substrate, a protection cap (36) provided on a light incident side of said solid-state image pickup element chip, said substrate has a thermal expansion coefficient substantially equal to that of said protection cap and the substrate and said protection cap are sealed with a sealing resin (40). Note that the material of the protective cap and the substrate of Hideki are the same as those disclosed by Applicant.

However, Hideki fails to teach a hollow space between the solid-state image pickup element chip and the protection cap. Applicant's admitted prior art teaches an image element chip (1) with pickup elements (7) with a protection cap (3) and a hollow space between the image element chip and the protection cap. Therefore, it would have been an obvious modification to someone with

ordinary skill in the art, at the time of the invention, to modify the structure as taught by Hideki to include a hollow space between the solid-state image pickup element chip and the protection cap, as clearly suggested by Applicant's admitted prior art, in order to provide a medium on which a vent hole can be produced and prevent damage to the device.

With regard to Claim 7, Hideki teaches a solid-state image pickup element chip (32) on which a plurality of solid-state image pickup elements are mounted, protection cap (36) on a light incident side of said solid-state image pickup element chip and adapted to protect said solid-state image pickup element chip, characterized in that said solid-state image pickup element chip is formed on a substrate (30) made of the same material as that of said protection cap and the substrate and said protection cap are sealed with a sealing resin (40).

However, Hideki fails to teach a hollow space between the solid-state image pickup element chip and the protection cap. Applicant's admitted prior art teaches an image element chip (1) with pickup elements (7) with a protection cap (3) and a hollow space between the image element chip and the protection cap. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Hideki to include a hollow space between the solid-state image pickup element chip and the protection cap, as clearly suggested by Applicant's admitted prior art, in order to provide a medium on which a vent hole can be produced and prevent damage to the device.

With regard to Claim 13, a further difference between Hideki and the claimed invention is, an optical low-pass or an infrared filter on the protection cap. It would have been an obvious modification to someone with rodnary skill in the art, at the time of the invention, to modify the structure as taught by Hideki to include an optical low-pass or an infrared filter on the protection cap, since it is a known practice in the art to use optical low-pass or infrared filters to limit the spatial frequency of incident light from a subject.

With regard to Claims 19 and 26, Hideki teaches a substrate (30) that is one of a glass substrate, ceramic substrate, metal substrate and resin substrate or a substrate formed by stacking some of the glass substrate, ceramic substrate, metal substrate and resin substrate.

With regard to Claims 20 and 27, Hideki teaches a sealing resin (40) that is selected from the group consisting of epoxy, acrylic and phenol-based resins.

Claims 14, 17, 18, 21, 24, 25, 28 and 29 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Hideki (Japanese Patent No. 08-241976) in view of Applicant's admitted prior art, as shown on figure 7, and further in view of Nakamura et.al. (U.S. Patent No. 5,138,145). With regard to Claim 14, as stated supra, Hideki and Applicant's admitted prior art essentially disclose the claimed invention but fail to show a light shielding layer at a periphery of the protection cap. Nakamura teaches an image sensor with simplified chip mounting that includes an

image pickup element chip formed on a substrate through a light-shielding layer (40) that comprises a flexible adhesive of resin. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Hideki and Applicant's admitted prior art, to include a solid-state image pickup element chip formed on the substrate through a light-shielding layer, as clearly suggested by Nakamura, in order to prevent malfunction of the device that may be caused by light reflection.

With regard to Claims 17 and 24, a further difference between Hideki and Admitted prior art and the claimed invention is, a flexible adhesive to adhere the solid-state image pickup element chip to the substrate. Nakamura teaches an image sensor with simplified chip mounting that includes an image pickup element chip which is adhered to a transparent substrate by a flexible adhesive (40) or resin. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Hideki and Admitted prior art, to include a flexible adhesive to adhere the solid-state image pickup element chip to the substrate, as clearly suggested by Nakamura, in order to improve the stability and the mounting of a chip over an insulating substrate.

With regard to Claims 18 and 25, a further difference between Hideki and Admitted prior art and the claimed invention is, a contact preventive member provided between each one of the plurality of solid-state image pickup elements and the sealing resin so the sealing resin will not come into

contact with each one of the plurality of solid-state image pickup elements. Nakamura teaches a protective layer (46) that serves as a contact preventive member provided between each one of the elements in the image pickup element chip and the sealing resin to prevent contact of the sealing resin and the image elements. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Hideki and Admitted prior art, to include a contact preventive member provided between each one of the plurality of solid-state image pickup elements and the sealing resin so the sealing resin will not come into contact with each one of the plurality of solid-state image pickup elements, as clearly suggested by Nakamura, in order to protect the circuit conductors so that current can flow into the image sensor.

With regard to Claims 21 and 28, as stated supra, Hideki and Applicant's admitted prior art essentially disclose the claimed invention but fail to show a light shielding layer between the substrate and the solid-state image pickup element chip. Nakamura teaches an image sensor with simplified chip mounting that includes an image pickup element chip formed on a substrate through a light-shielding layer (40) that comprises a flexible adhesive of resin. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Hideki and Applicant's admitted prior art, to include a light shielding layer between the substrate and the solid-state image pickup element chip,

as clearly suggested by Nakamura, in order to prevent malfunction of the device that may be caused by light reflection.

With regard to Claim 29, a further difference between Hideki and Applicant's admitted prior art is, a light shielding layer formed of a light shielding and flexible adhesive. Nakamura teaches an image sensor with simplified chip mounting that includes an image pickup element chip formed on a substrate through a light-shielding layer (40) that comprises a flexible adhesive of resin. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Hideki and Applicant's admitted prior art, to include a light shielding layer formed of a light shielding and flexible adhesive, as clearly suggested by Nakamura, in order to prevent malfunction of the device that may be caused by light reflection.

***Response to Arguments***

4. Applicant's arguments with respect to claims 1, 7 and 13-29 have been considered but are moot in view of the new ground(s) of rejection.

*Conclusion*

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO/AU 2815

8/6/02

ALLAN R. WILSON
PRIMARY EXAMINER